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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/071,013	02/08/2002	Gang Zha	00-SZ-106	8843
30422	7590	05/11/2004	EXAMINER	
STMICROELECTRONICS, INC. MAIL STATION 2346 1310 ELECTRONICS DRIVE CARROLLTON, TX 75006			MOTTOLA, STEVEN J	
			ART UNIT	PAPER NUMBER
			2817	

DATE MAILED: 05/11/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	10/071,013	ZHA ET AL.	
	<b>Examiner</b>	<b>Art Unit</b>	
	Steven J. Mottola	2817	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

1) Responsive to communication(s) filed on 11 February 2004.  
 2a) This action is **FINAL**.                    2b) This action is non-final.  
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

4) Claim(s) 1-15 is/are pending in the application.  
 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.  
 5) Claim(s) 10 is/are allowed.  
 6) Claim(s) 1-9 and 11-15 is/are rejected.  
 7) Claim(s) \_\_\_\_\_ is/are objected to.  
 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

9) The specification is objected to by the Examiner.  
 10) The drawing(s) filed on 2-11-04 is/are: a) accepted or b) objected to by the Examiner.  
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
 a) All    b) Some \* c) None of:  
 1. Certified copies of the priority documents have been received.  
 2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

1) Notice of References Cited (PTO-892)  
 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)  
 3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
 Paper No(s)/Mail Date \_\_\_\_\_.  
 4) Interview Summary (PTO-413)  
 Paper No(s)/Mail Date. \_\_\_\_\_.  
 5) Notice of Informal Patent Application (PTO-152)  
 6) Other: \_\_\_\_\_.

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Claims 5-9,12-13 and 15 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 5 & 6 refer to the fifth and sixth transistors as being in a current mirror configuration when as the applicant has stated in the preamendment filed February 11, 2004 and as shown in the figures as Q5 & Q6, they are not. Regarding claim 15, there is no antecedent basis for "the negative input terminal".

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-4,11 and 14 are rejected under 35 U.S.C. 102(b) as being anticipated by Nishioka et al.

Refer to fig. 3 of Nishioka et al. Treating independent claims 1 & 14 first, differential pair Q6,Q7 may be read as the input stage claimed while Q4,Q5 may be read as the output stage claimed generating two signals of equal current (see equation 2 of col. 2, where IA and IO are the output currents of Q4 and Q5 respectively). The signal from Q4 may be used as a feedback to the input stage (Q7) and the signal from Q5 may be used as the circuit output. Transistors Q8,Q9 form a current mirror and may be read as the gain stage claimed. Regarding the last two paragraphs of claim 14, a voltage potential Vcc-Vee is applied across the amplifier and a resistor R4 is connected between the first output (that of Q4) and the potential Vcc. Regarding claim 2, the pair

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Q6,Q7 may be read as the first and second transistors claimed while current source 22 may be read as the like element claimed. The interconnections are as claimed.

Likewise, in re claims 3-4, Q8,Q9 may be read as the third and fourth transistors claimed and the interconnections are as claimed. Regarding claim 11, the input signal is provided by applying a signal Vi (read as the first potential of the claim) between an input terminal and ground (read as the second potential of the claim) and coupling the other input terminal to the output of Q4 (read as the first output). The resistive element claimed may be read as resistor R4 as it is connected between the collector of Q4 (first output) and Vcc (read as the third potential of the claim).

Claim 10 is allowed, as Nisioka et al. do not show a resistor that may be read on the first resistor claimed.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven J. Mottola whose telephone number is 571-272-1766. The examiner can normally be reached on M-Th from 8 to 5.

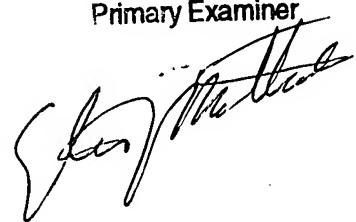
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert J. Pascal, can be reached on 571-272-1769. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should

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you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Steven J. Mottola  
Primary Examiner

A handwritten signature in black ink, appearing to read "Steven J. Mottola".